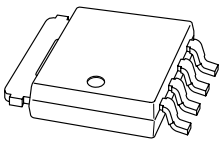


# PH2625L

## N-channel TrenchMOS™ logic level FET

Rev. 02 — 24 February 2005 Preliminary data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Optimized for use in DC-to-DC converters
- Low threshold voltage
- Very low switching and conduction losses
- Low thermal resistance.

### 1.3 Applications

- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- Notebook computers.

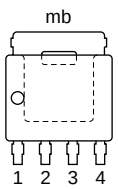
### 1.4 Quick reference data

- $V_{DS} \leq 25$ V
- $Q_{gd} = 7.3$ nC (typ)
- $R_{DSon} \leq 2.8$ mΩ ($V_{GS} = 10$ V)
- $I_D \leq 100$ A
- $Q_{g(tot)} = 32$ nC (typ)
- $R_{DSon} \leq 4.1$ mΩ ($V_{GS} = 4.5$ V).

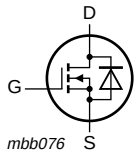
## 2. Pinning information

**Table 1: Pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1, 2, 3 | source | | |
| 4 | gate | | |
| mb | mounting base; connected to drain | | |




**SOT669 (LFPAK)**




PHILIPS

## 3. Ordering information

**Table 2: Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PH2625L | LFPAK | plastic single-ended surface mounted package; 4 leads | SOT669 |

## 4. Limiting values

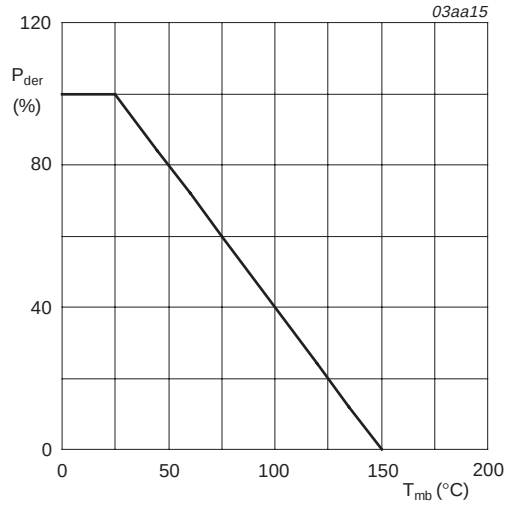
**Table 3: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C | | - | 25 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | | - | 25 | V |
| $V_{GS}$ | gate-source voltage | | | - | ±20 | V |
| $I_D$ | drain current (DC) | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; Figure 2 and 3 | | - | 100 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 10 V; Figure 2 | | - | 63 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; Figure 3 | | - | 300 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Figure 1 | | - | 62.5 | W |
| $T_{stg}$ | storage temperature | | | –55 | +150 | °C |
| $T_j$ | junction temperature | | | –55 | +150 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source (diode forward) current (DC) | $T_{mb}$ = 25 °C | | - | 52 | A |
| $I_{SM}$ | peak source (diode forward) current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs | | - | 156 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D$ = 71 A; $t_p$ = 0.1 ms; $V_{DD}$ ≤ 25 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; starting at $T_j$ = 25 °C | | - | 250 | mJ |
| $E_{DS(AL)R}$ | repetitive drain-source avalanche energy | unclamped inductive load; $I_D$ = 7.1 A; $t_p$ = 0.01 ms; $V_{DD}$ ≤ 25 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V | [1] [2] | - | 2.5 | mJ |

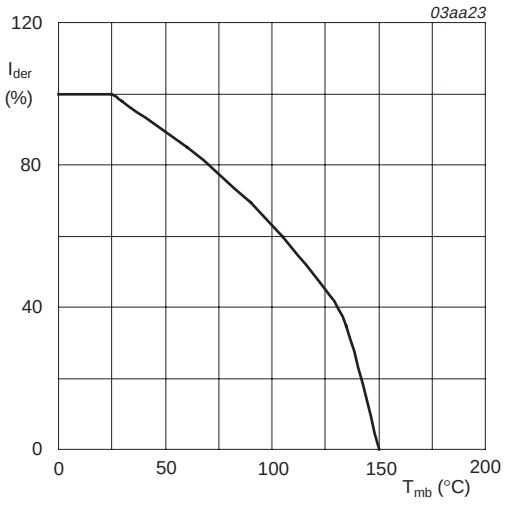
[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



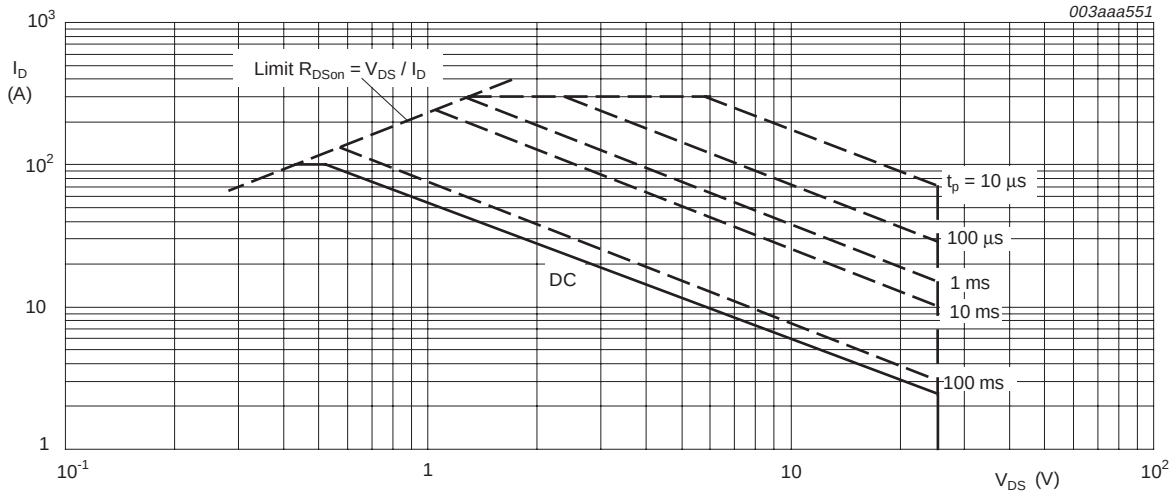

$$P_{der} = \frac{P_{tot}}{P_{tot(25\ ^\circ C)}} \times 100\ \%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature**




$$I_{der} = \frac{I_D}{I_{D(25\ ^\circ C)}} \times 100\ \%$$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C; $I_{DM}$ is single pulse; $V_{GS}$ = 10 V

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 4: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | Figure 4 | - | - | 2 | K/W |

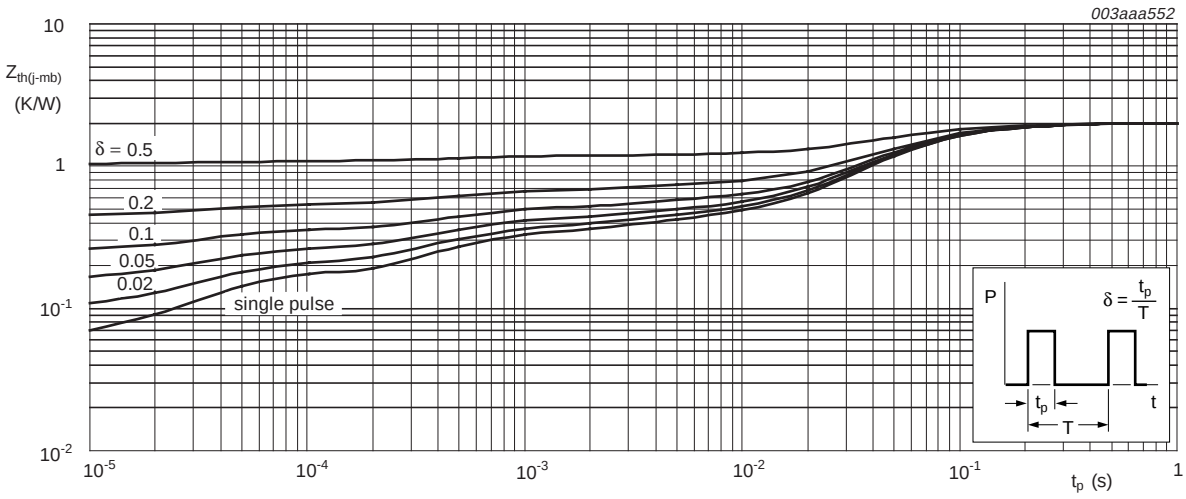


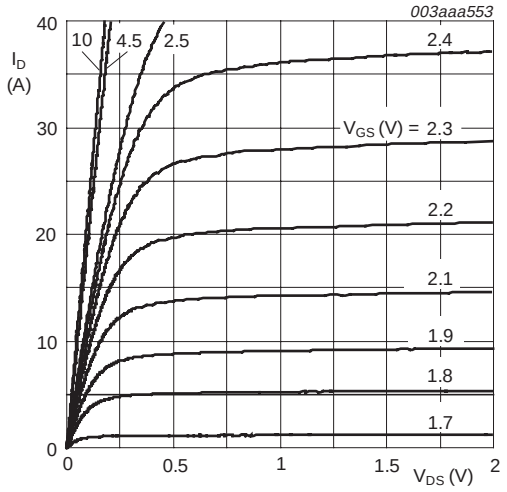

**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 5: Characteristics**

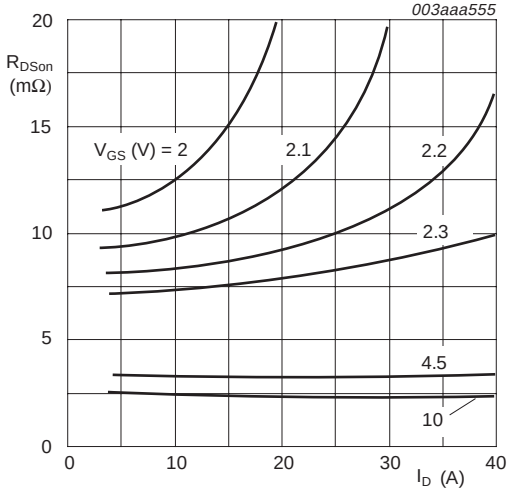
*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V | 25 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; Figure 9 and 10 | | | | |
| | | $T_j$ = 25 °C | 1 | 1.5 | 2 | V |
| | | $T_j$ = 150 °C | 0.5 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 2.2 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | 0.06 | 1 | µA |
| | | $T_j$ = 150 °C | - | - | 500 | µA |
| $R_G$ | gate resistance | f = 1 MHz | - | 1.5 | - | Ω |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±16 V; $V_{DS}$ = 0 V | - | 10 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; Figure 6 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 2 | 2.8 | mΩ |
| | | $T_j$ = 150 °C | - | 3.2 | 4.3 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; Figure 6 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 3 | 4.1 | mΩ |
| | | $T_j$ = 150 °C | - | 4.8 | 6.6 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 12 V; $V_{GS}$ = 4.5 V; Figure 11 and 12 | - | 32 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 9.6 | - | nC |
| $Q_{gs1}$ | pre-$V_{GS(th)}$ gate-source charge | | - | 6 | - | nC |
| $Q_{gs2}$ | post-$V_{GS(th)}$ gate-source charge | | - | 3.6 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 7.3 | - | nC |
| $V_{plat}$ | plateau voltage | | - | 2.2 | - | V |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 4.5 V | - | 26 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 12 V; f = 1 MHz; Figure 13 and 14 | - | 4308 | - | pF |
| $C_{oss}$ | output capacitance | | - | 1137 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 439 | - | pF |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 0 V; f = 1 MHz | - | 4830 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 12 V; $R_L$ = 0.48 Ω; $V_{GS}$ = 4.5 V; $R_G$ = 4.7 Ω | - | 41 | - | ns |
| $t_r$ | rise time | | - | 52 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 67 | - | ns |
| $t_f$ | fall time | | - | 30 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; Figure 15 | - | 0.85 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = –100 A/µs; $V_{GS}$ = 0 V; $V_R$ = 25 V | - | 47 | - | ns |
| $Q_r$ | recovered charge | | - | 22 | - | nC |



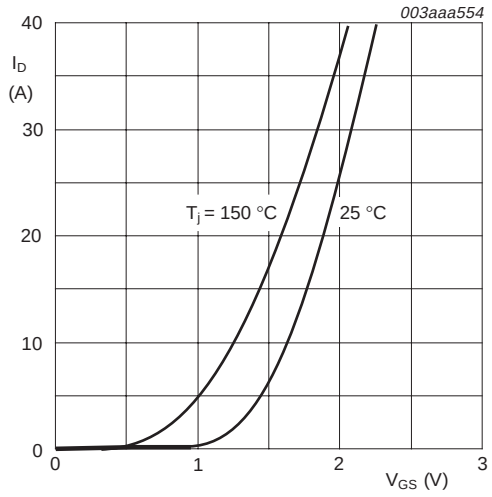

$T_j$ = 25 °C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



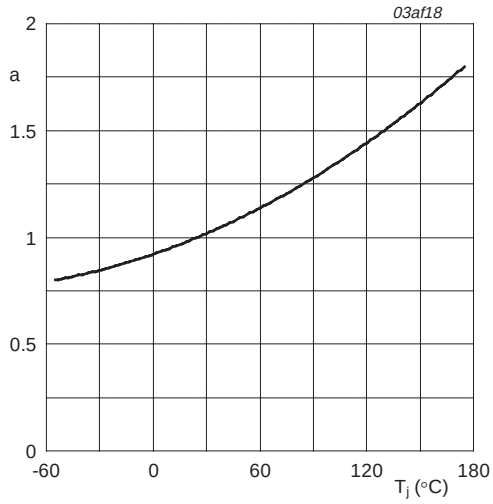

$T_j$ = 25 °C

**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**



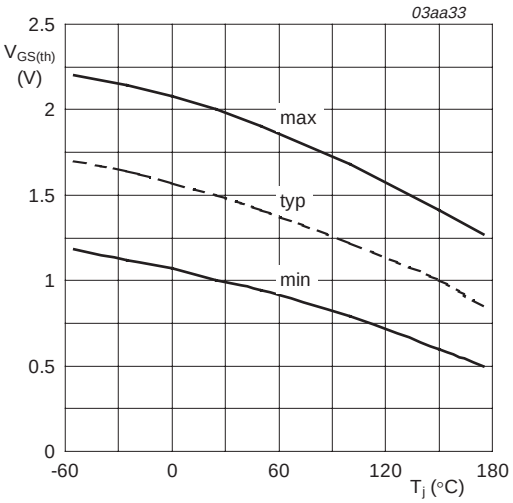

$T_j$ = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



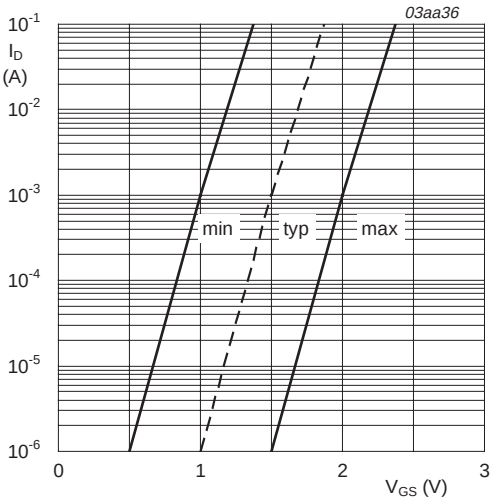

$$a = \frac{R_{DSon}}{R_{DSon(25\,^{\circ}C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



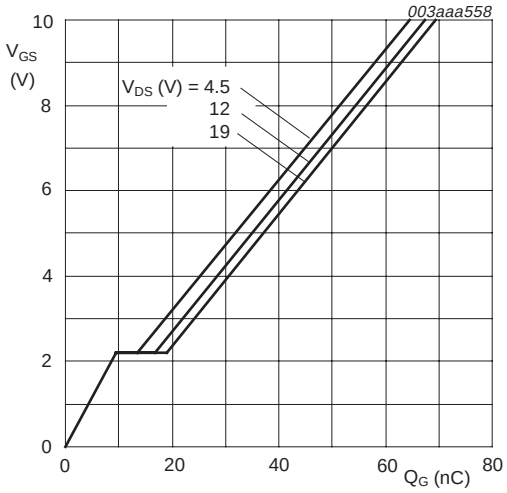

$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**




$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**




$I_D$ = 25 A; $V_{DS}$ = 4.5 V, 12 V and 19 V

**Fig 11. Gate-source voltage as a function of gate charge; typical values**

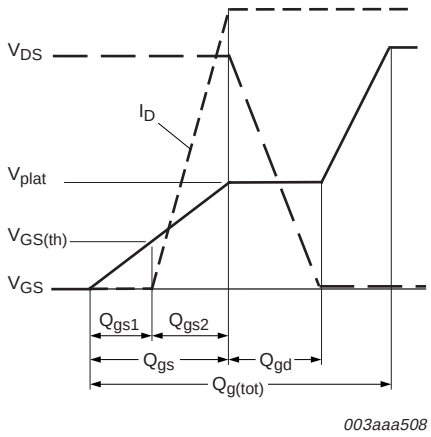
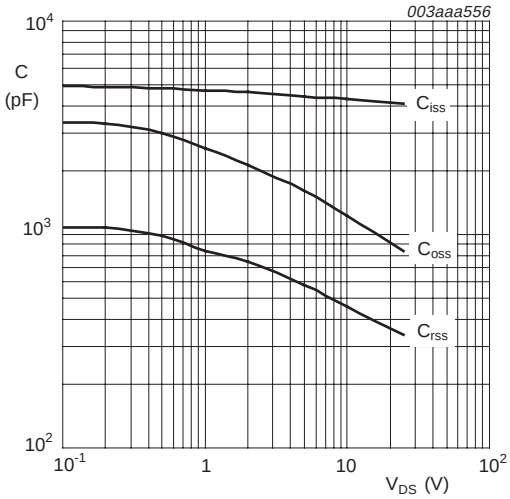
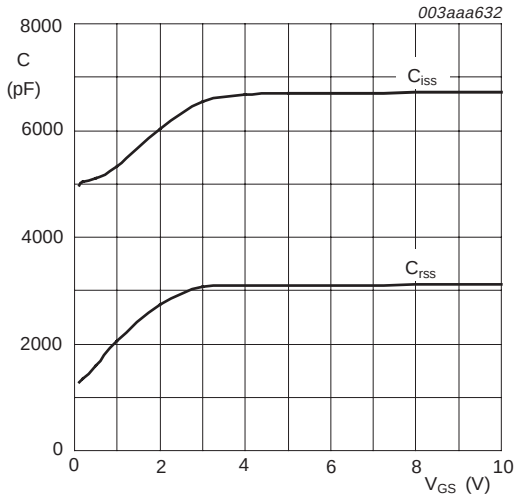



**Fig 12. Gate charge waveform definitions**



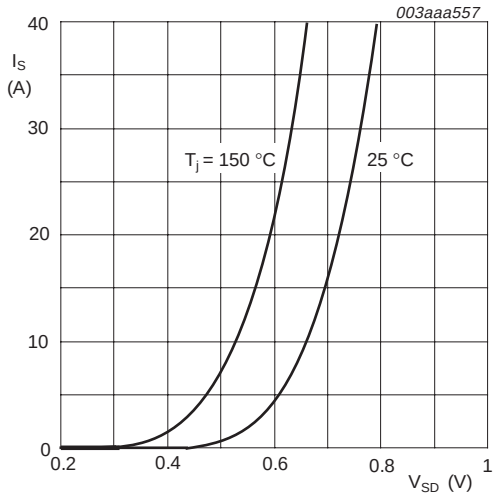

$V_{GS}$ = 0 V; f = 1 MHz

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**




$V_{DS}$ = 0 V; f = 1 MHz

**Fig 14. Input and reverse transfer capacitances as a function of gate-source voltage; typical values**

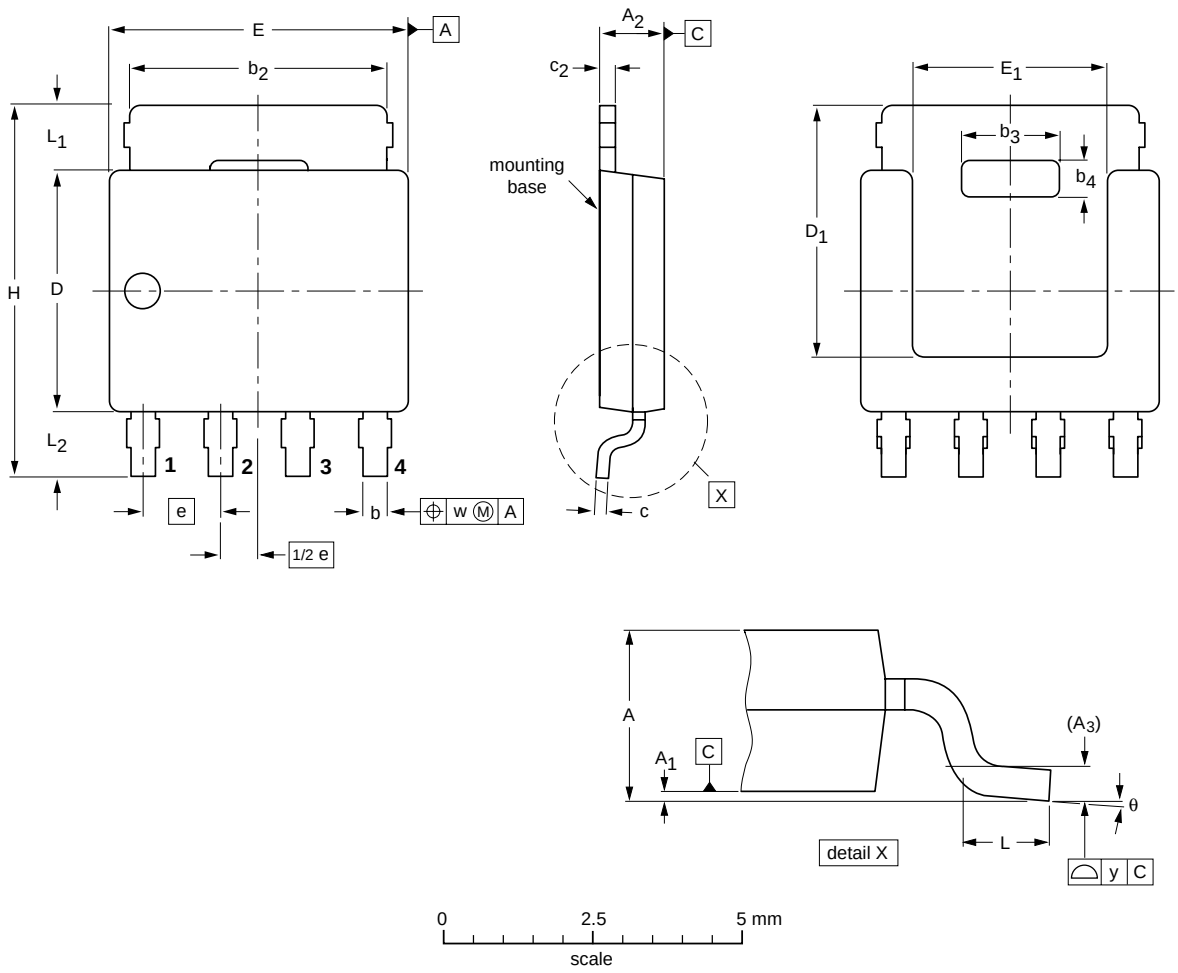



$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

## 7. Package outline

**Plastic single-ended surface mounted package (LFPAK); 4 leads** **SOT669**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | $D^{(1)}$ | $D_1^{(1)}$ max | $E^{(1)}$ | $E_1^{(1)}$ | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.20<br>1.01 | 0.15<br>0.00 | 1.10<br>0.95 | 0.25 | 0.50<br>0.35 | 4.41<br>3.62 | 2.2<br>2.0 | 0.9<br>0.7 | 0.25<br>0.19 | 0.30<br>0.24 | 4.10<br>3.80 | 4.20 | 5.0<br>4.8 | 3.3<br>3.1 | 1.27 | 6.2<br>5.8 | 0.85<br>0.40 | 1.3<br>0.8 | 1.3<br>0.8 | 0.25 | 0.1 | 8°<br>0° |

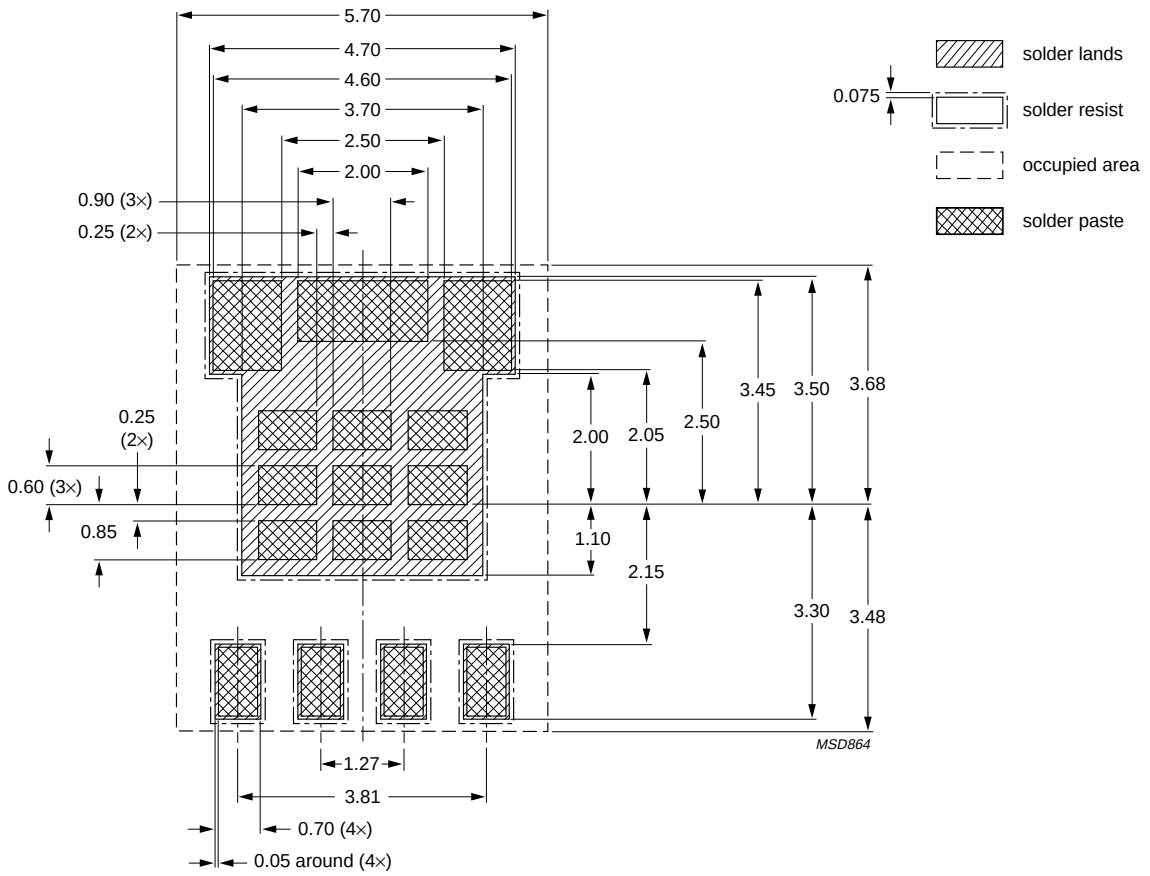
**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~03-09-15~~<br>04-10-13 |

**Fig 16. Package outline SOT669 (LFPAK)**

## 8. Soldering




All dimensions in mm

**Fig 17. Optimized soldering footprint SOT669 (LFPAK)**

## 9. Revision history

**Table 6: Revision history**

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|---|---|---|---|---|---|
| PH2625L_2 | 20050224 | Preliminary data sheet | - | 9397 750 14324 | PH2625L-01 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.<br>• $R_{DSon}$ data revised in Section 1.4 “Quick reference data” and Section 6 “Characteristics” | | | | |
| PH2625L-01 | 20040428 | Preliminary data sheet | - | 9397 750 12306 | - |

## 10. Data sheet status

| Level | Data sheet status [1] | Product status [2] [3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 11. Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information —** Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 12. Disclaimers

**Life support —** These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes —** Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## 13. Trademarks

**TrenchMOS —** is a trademark of Koninklijke Philips Electronics N.V.

## 14. Contact information

**For additional information, please visit: http://www.semiconductors.philips.com**

**For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com**

## 15. Contents





**Date of release: 24 February 2005**
**Document number: 9397 750 14324**

**Published in The Netherlands**